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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,175	03/31/2004	Fernando Gonzalez	MI22-2536	3055

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EXAMINER	
DIAZ, JOSE R	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/817,175	GONZALEZ ET AL.
	Examiner	Art Unit
	José R. Díaz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4 and 6-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4 and 6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/04 & 10/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 4 and 6-15 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 5-12 and 14-15 of copending Application No. 10/817,704. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the copending application recites the invention claimed in the instant application. For example:

Regarding claim 4, claim 5 of the copending application teaches a method of forming semiconductor circuitry, comprising:

providing a monocrystalline silicon wafer (see claim 2, lines 3-4);

forming a mask which covers a first portion of the wafer and leaves a second portion uncovered (see claim 2, lines 5-6);

forming a recess in the uncovered portion (see claim 2, line 9);

at least partially filling the recess with a semiconductive material that comprises at least 1 atomic percent of an element other than silicon (see claim 2, lines 13-15);

removing the mask (claim 2, line 16);

forming a first semiconductor circuit component over the first portion of the wafer (see claim 2, line 19);

forming a second semiconductor circuit component over the semiconductive material that is at the second elevational height (see claim 2, lines 21-22).

wherein the wafer includes an insulative material over the monocrystalline silicon wafer, and a monocrystalline silicon mass over the insulative material, wherein the recess is formed through the monocrystalline silicon mass and insulative material (see claim 5, lines1-6).

Regarding claims 6-12, claims 6-12 of the copending application teaches a semiconductive material consisting of one of a III/V compound semiconductive material, a semiconductive material consisting of Si and at least 1% carbon, and a semiconductive material consisting of Si and about 1% to 20% Ge.

Regarding claim 13, claim 2, lines 11-15 of the copending application teaches the step of providing an insulative material spacer along a sidewall of the recess; and wherein the at least partially filling the recess with the semiconductor material comprises providing the semiconductive material along the insulative material spacer.

Regarding claim 14, claims 14, lines 1-2 of the copending application teaches a spacer comprising silicon nitride.

Regarding claim 15, claims 15, lines 1-2 of the copending application teaches a spacer comprising silicon oxide.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 4 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US Pat. No. 6,555,891 B1) in view of Nakai et al. (US Pat. No. 5, 891, 265).

Regarding claim 4, Furukawa et al. teaches a method of forming semiconductor circuitry, comprising:

providing a SOI substrate comprising a bulk monocrystalline silicon structure (12), an insulative material (16) on the bulk monocrystalline silicon structure, and a silicon mass (15) over the insulative material (see fig. 1 and col. 3, lines 1-12);

forming a mask (17) which covers a first portion of the substrate (portion outside the trench) and leaves a second portion uncovered (portion in which the trench is formed. See fig. 3);

forming a recess (20) in the uncovered portion (see fig. 3);

at least partially filling the recess with a semiconductive material (24) that comprises at least 1 atomic percent of an element (Ge) other than silicon (see fig. 5, and col. 4, lines 57-65);

removing the mask (170 (see fig. 8);

forming a first semiconductor circuit component over the first portion of the wafer (outside the trench) (see col. 2, lines 1-2);

forming a second semiconductor circuit component over the semiconductive material (24) that at least partially fills the recess (see col. 1, line 67 and col. 2, line 1);

wherein the recess (20) is formed through the silicon mass (15) and to the insulative material (16) (see fig. 3).

However, Furukawa et al. fails to teach an SOI substrate having a monocrystalline silicon mass over the insulative material.

Nakai et al. teaches that it is well known in the art to form an SOI substrate having a monocrystalline silicon (11) over the insulative material (3) (see fig. 5D, col. 9, lines 25-26 and col. 10, lines 17-21).

Furukawa et al. and Nakai et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an SOI having a monocrystalline silicon mass over the insulative material. The motivation for doing so, as is taught by Nakai et al., is reducing the junction leak current between source and drain, resulting in reduction of power consumption (col. 8, lines 50-52). Therefore, it would have been obvious to combine Nakai et al. with Furukawa et al. to obtain the invention of claims 4 and 13-15.

Regarding claim 13, Furukawa et al. teaches the step of providing an insulative material spacer (22) along a sidewall of the recess (see fig. 4); and wherein the at least partially filling the recess with the semiconductor material (24) comprises providing the semiconductive material along the insulative material spacer (see fig. 5).

Regarding claim 14, Furukawa et al. teaches a spacer comprising silicon nitride (col. 4, lines 11-15).

Regarding claim 15, Furukawa et al. teaches a spacer comprising silicon oxide (col. 4, lines 11-15).

6. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US Pat. No. 6,555,891 B1) in view of Nakai et al. (US Pat. No. 5, 891, 265), and further in view of Shimbo (US Pat. No. 5,036,374).

Regarding claims 6-10, a further difference between the prior art and the present invention is the step of forming the semiconductive material that at least partially fills the recess consisting of essentially of one of a III/V compound semiconductive material and a silicon and at least 1% carbon material. Shimbo teaches that it is well known in the art to substitute the SiGe semiconductor material with a III/V compound semiconductive material or SiC (see col. 3, lines 49-51).

Shimbo, Nakai et al. and Furukawa et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further form the semiconductive material of one of a III/V compound semiconductive material and a silicon and at least 1% carbon material. The motivation for further doing so, as is taught by Shimbo, is increasing the speed of the device by increasing the electron mobility in the channel region (col. 3, lines 44-46). Therefore, it would have been obvious to further combine Shimbo with Nakai et al. and Furukawa et al. to obtain the invention of claims 6-10.

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US Pat. No. 6,555,891 B1) in view of Nakai et al. (US Pat. No. 5, 891, 265), and further in view of Imai et al. (JP 09219524 A).

Regarding claims 11-12, a further difference between the prior art and the present invention is the step of forming the semiconductive material that at least partially fills the recess consisting of essentially of Si and Ge, with the Ge being present to an atomic concentration of about 20%. Imai et al. teaches that it is well known in the art to form a semiconductive material (4) that at least partially fills the recess (20) consisting essentially of Si and Ge (abstract), with the Ge being present to an atomic concentration of about 20% (see paragraph [0019]).

Imai et al., Nakai et al. and Furukawa et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further form the semiconductive material of essentially of Si and Ge, with the Ge being present to an atomic concentration of about 20%. The motivation for further doing so, as is taught by Imai et al., is forming a high speed and highly efficient integrated transistor (abstract). Therefore, it would have been obvious to further combine Imai et al. with Nakai et al. and Furukawa et al. to obtain the invention of claims 11-12.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/21/05

José R. Díaz
Examiner
Art Unit 2815